

G-500 Sushant Lok Phase 2  
Sector 57  
Pin-122003  
+91-9467597670

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## JYOTI YADAV

**CAREER OBJECTIVE** To continue to grow and excel professionally

### PERSONAL PROFILE

**Name** : Jyoti Yadav  
**Sex** : Female  
**D.O.B** : 27 January 1993  
**Father's name** : Gulab Singh  
**Permanent Address** : G-500 Sushant Lok Phase 2 ,Sector 57, Pin-122003  
**Phone no.** : 9467597670  
**Nationality** : Indian

### SKILLS & ABILITIES

Languages Known: English , Hindi  
Excellent Presentation and motivation skills  
Strong analytical , logical and mathematical skills  
Ability to provide quality Knowledge  
Programming Languages: Assembly 8086 Microprocessor , C, C++  
Hardware description languages – VHDL , Verilog  
Tools- Matlab , ORCAD , Multisim , Labview, Modelsim Student Edition

### WORK EXPERIENCE

3<sup>rd</sup> August 2015 – Present  
**Scientist 'B'** in Centre of Airborne Systems, Bangalore , **Defense Research and Development Organization**

### EDUCATION

**NIT KURUKSHETRA – B.TECH IN ECE**  
2011-2015  
**CGPA- 9.0**  
Best SGPA – 9.3019  
**KENDRIYA VIDYALYA N.S.G MANESAR , GURGAON**  
**AISSCE- 93.6 %**  
**AISSE - 92.2%**

**INTERNSHIPS &  
TRAINING**

**DEFENCE R&D ORGANISATION- LASER SCIENCE AND TECHNOLOGY CENTRE**

Designing and implementation of pre-amplifier and a simple GUI for Nd:Yag laser

June 13<sup>th</sup>, 2014 to July 24<sup>th</sup>, 2014

The problem statement was to make a pre-amplifier with minimum bandwidth of 10 MHz and variable gain using AD829 . The width of the signal also have to be preserved during the process . Along with provide amplification , the amplifier also removed ringing effect due to noise in the scattered signal. The GUI for Nd: YAG laser was developed using LABVIEW software. In this Start and Stop functions were implemented for Nd:YAG laser.

**DUCAT GURGAON – VERILOG COURSE**

May 28<sup>th</sup>, 2013 to July 12<sup>th</sup>, 2013

I learned Verilog under the guidance of Mr. Piyush and worked on two projects- Snake and ladder game using Verilog and Digital clock using Verilog and was able to successfully complete both of them in time.

**SPARSHA LEARNING TECHNOLOGIES PRIVATE LIMITED STEP,  
INDIAN INSTITUTE OF TECHNOLOGY, KHARAGPUR, WEST BENGAL**

March 4<sup>th</sup>, 2013 to Aug 4<sup>th</sup>, 2013.

This was a paid online internship and my job as an internee was to promote DoCircuits - tool for circuit simulation. I provided material to be posted on their Facebook page DoCircuits and uploaded sample circuits using their tool, which can be used as examples by users on their website <http://www.docircuits.com/>

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I, hereby, declare that the above information provided by me is true to the best of my knowledge and belief.

Dated: November 23, 2015

**(JYOTI YADAV)**