Suman
Mob: +91-9518608739
H. No. 33, Vashudev Pura,
Near Sapient Public School, Pinjore ,134102,
Email: su.chahar@gmail.com

# Assistant Professor Applicant (Electronics Science)

**PROFILE:**

- Highly committed to teaching, self-motivated Ph.D. candidate with demonstrated teaching experiences during my Ph.D. tenure at NIT Srinagar and research expertise in Semiconductor devices, Microelectronics, Analog & Digital Electronics, Microprocessor, Power MOS devices and Control system.
- In all my teaching activities, I incorporate techniques, like problem solving exercises and brainstorming, to increase student interaction and to promote active learning.
- Fab. Process: Thin film deposition using Vacuum system, wafer cleaning, photolithography oxidation (wet, dry).
- Rich experience in modeling and computer simulation using ATLAS SILVACO, Fuzzy, PLC, ANSYS, MATLAB, Scilab, VHDL, PSpice
- Worked-on Platforms like Windows Xp/Vista/Window7, Window 8, 8.1, 10 & LINUX.
- Computer skills: HTML, CSS, Microsoft Azure, C & Assembly
- Strong interpersonal skills

**EDUCATION:**

**National Institute of Technology, Srinagar, India**
Ph.D. Power Semiconductor MOSFET devices, 2013- 2019

**Kurukshetra University, Kurukshetra, India**
Master's in technology (MTech.) in Instrumentation, 2009-11, (CGPA: 7.65/10.0)
Master's in Sciences (M.Sc.) in Electronic, 2007-09, (Marks: 1606/2500)
Bachelor's in Sciences (B.Sc.) in Electronic Equipment's, 2004-07, (Marks: 925/1450)

**RESEARCH INTERESTS:**

- Modeling, Simulation and fabrication of semiconductor Devices and circuits.
- Modeling, Simulation and fabrication of Power Devices and circuits.
- Study of Semiconductor devices in RF applications with employing different materials such as SiGe, GaN, GaAs etc.

**TEACHING EXPERIENCES:**

- 2 years teaching experience from Adarsh Senior Secondary School (April 2019-April 2020, January 2012 - February 2013)

**ENGINEERING RESEARCH EXPERIENCE:**

**National Institute of Technology**, Srinagar, India
**Ph.D. Candidate**, 2013-2019
**Guide:** Prof G. M. Rather
•*Dissertation - Investigation Study of SG-LDMOS and DG-LDMOS Devices for RF Applications*

The present work had been taken up to investigate semiconductor devices for RF power applications. A detailed literature survey was carried out about devices used for RF power applications. The literature survey revealed that LDMOS is the most suitable device for RF power circuits. Accordingly LDMOS was taken up for further study and examination. The investigation has been carried out through simulations and analytical modeling. The parameters like BV, $R_{ON}$, $g_m$, DIBL $f_T$, $f_{MAX}$ etc. were analyzed. These parameters have been taken from the reference paper. The research study was carried out in two phases. In first phase the AC and DC behavior of SG-LDMOS device was examined using analytical modeling and simulation studies. The effects of channel length and gate length were observed on the parameters of interest i.e. BV, $R_{ON}$, $g_m$, DIBL $f_T$ and $f_{MAX}$ etc. The study revealed that SG-LDMOS is a right device for RF power applications up to roughly 10GHz range. It was also observed that there exists a tradeoff among some parameters like BV, $R_{ON}$ and frequency. In order to achieve the best possible results the structure of SG-LDMOS

has been refined by different people using different techniques. In this direction, to achieve the better RF range, a new DG-LDMOS was proposed. The device employs two gates for control of operation of device. The proposed device was also investigated for the parameters like BV, $R_{ON}$, $g_m$, DIBL $f_T$, $f_{MAX}$ using analytical and simulation techniques.
From the study following observations were made:

(i) DG-LDMOS offers higher BV than SG-LDMOS
(ii) It has low RON as compared to SG-LDMOS
(iii) It has higher fT and fMAX as compared to SG-LDMOS
(iv) Second gate helps in reduction of peak electric field near the drain end hence BV enhanced, improved gm and reduce go and a desirable Vth.
(v) DG-LDMOS device reduces the sharp peaks in capacitance and has lower parasitic capacitance hence this device can operate at higher frequency.
(vi) Above all the DG-LDMOS exhibited higher current drive capability without degrading the BV, improvement in gm, Rout, BV, Intrinsic gain, fT and fMAX, reduced on-resistance and go. Hence this device can be used for RF power amplifier.

**I.I.E (USIC), Kurukshetra University, Kurukshetra**, India
**Guide:** Associate Prof. Dinesh Singh Rana
•*Dissertation Project - Automation of paper mill digester using FLC & PLC – A simulation Approach*
*Duration: 6 months, Jan-July 2011*
Developed a new architecture for batch digester. The functioning of batch digester was automated through Fuzzy logic controller & PLC (RS logic 500). The new architecture for batch system has been designed in modular fashion thereby providing future incremental system growth. Batch digester provided complete scheduling, process control and optimization to improve digester production through increased blows, to reduce operational costs and quality variance by maintaining consistent and stable kappa.

**Central Electronics Engineering Research Institute (CEERI), Pilani, Rajasthan,** India
**Guide:** Dr. R.K. Sharma
*Dissertation Project - Thermal & Structural analysis of helix electron gun of TWT*
*Duration: 7 months, June-Dec 2008*

For broadband satellite communication applications, the Travelling Wave Tube (TWT) are mainly employed. TWTs are used because of their excellent reliability, high power, large bandwidth and small size. TWT amplifier is an electronics device used to produce high power radio frequency signals. It is one of the most critical and expensive components of the satellite. The electron gun is a vital component of a travelling wave tube.
In the present work the thermal and structural aspects of electron gun of HELIX TWT were analyzed using ANSYS package in order to simulate the performance under operating conditions. The input geometrics for the package were generated from the given dimensions of HELIX-TWT. In the geometry generation, the lines and areas were created using key points with reference to a coordinate axis. The thermal simulation studies included steady state temperature distribution & transient temperature distribution on 2D and 3D geometry. The thermal analysis was used for proper management of cathode surface. The structural analysis was used for proper dimension. The structural analysis analyzed the thermal stresses at different points of electron gun.

**MAJOR COURSES:**

- Integrated Circuit Engineering-Silicon Processing
- Semiconductor Devices for IC
- Solid State Physics
- Analog and Digital Electronic Devices and Circuits
- Communication System
- Advanced Digital System Design
- Microwave Engineering
- Physics of semiconductor devices
- Embedded system
- Measurements
- Network Theory

**PUBLICATIONS:**

- **IEEE Transactions of Electron Devices**, "The Effect of Shallow Trench Isolation and Sinker on the Performance of Dual Gate LDMOS Device,"Vol.66, Issue:1, PP.585-591, Jan 2019, ISSN No:1557-9646.
- Journal of Computational Intelligence and Electronic Systems (JCIES), "Effect of Scaling Parameters of Laterally Double Diffused Metal Oxide Semiconductor Device on Drain Induced Barrier Lowering" Vol. 5, Issue 1, PP. 58-62, March 2016.
- International Journal of Engineering Applied Sciences and Technology (IJEAST) "THE EFFECT OF CHANNEL AND GATE LENGTH OF LDMOS DEVICE ON ITS PERFORMANCE" Vol. 1, Issue 4, PP. 62-68, 2016, ISSN No. 2455-2143.
- International Journal of Latest Research in Engineering and Technology (IJLRET) "Analysis and Design of a Low Voltage Si LDMOS Transistor" Vol. 1, Issue 3, PP 65-69, Aug 2015 ISSN No: 2454-5031.
- International Journal of Engineering Applied Sciences and Technology (IJEAST), "Impact of Channel Length on the Performance of Dual Gate LDMOS" (**accepted**).
- **IEEE Transactions of Electron Devices**, "Study of Characteristics Behavior of DG-LDMOS Device", (under communication).
- **Semiconductor Science and Technology**," Analytical Study of characteristics behavior SG-LDMOS Device" (under communication)**.**

**CONFERENCES / PRESENTATIONS:**

- IEEE-International Conference on Electrical, Electronics, Computers, Communication, Mechanical and Computing (EECCMC) at Priadarshini Engineering College, Tamil Nadu Vellore, "Simulation Investigation of Single Gate-Laterally Double Diffused MOSFET for RF Applications," 28-29th Jan 2018.
- IEEE-International Conference on current Trends in Converging Technologies (ICCTCT 2018), SVS College of Engineering, Coimbatore, "Investigation of Characteristic Features of Dual Gate-LDMOS through Simulations", 1-3 March 2018.
- IEEE Seventh India International Conference on Power Electronics (IICPE-2016), "The Performance of Dual Gate LDMOS Device with STI & Sinker" Nov 17-19, 2016.
- 18th International Workshop on The Physics of Semiconductor Devices (18th IWPSD), IISc, Bangalore, India, "Effect of Gate and Channel Length of LDMOS Device on DIBL", December 7-10, 2015.
- IEEE-International Conference on Electrical, Electronics, Signals, Communication and Optimization (EESCO)-2015 at Vignan's Institute of Information Technology, Visakhapatnam, "The Impact of Gate and Channel Length of a Si LDMOS Transistor on its On Resistance and Breakdown Voltage" 24th-25th January 2015
- "Diamond Jubilee seminar on Leveraging ICT for Growth and Development of J&K (LICT-J&K 2013) on 13-14 September 2013" abstract, at NIT, Srinagar

**WORKSHOPS:**

- Scientific and Technical Documentation Using "Latex" workshop at National Institute of Technology, Srinagar, June 2016.
- Open Source Technologies through ICT at National Institute of Technology, Srinagar, January 2016.
- Workshop on PLC & SCADA as a part of National Technology Awareness Campaign, conducted by Codex Design Services, at National Institute of Technology, Srinagar, June 2015.
- INUP Nano fabrication workshop at Indian Institute of Science (IISC) at Bangalore, 28-30th January 2015.

- 18th International Workshop on The Physics of Semiconductor Devices (18th IWPSD), IISc, Bangalore, Dec 2015.

**MEMBERSHIPS:**

- Associate Member of The Institution of Electronics & Telecommunication Engineers (IETE).
- Member of IEEE.
- Member of IET.

**REFERENCES:**

- Dr. G.M. Rather - Professor, ECE department, National Institute of Technology, Srinagar, Contact No. +91-9419076741.
- Dr.Najib-Udin-Shah – Professor, ECE department, National Institute of Technology, Srinagar, Contact No. +91-9906666033.
- Dr. Dinesh Singh Rana -Professor, I.I.E (USIC). Kurukshetra University, Kurukshetra, Contact No. +91-9466045776.

**EXTRA ACTIVITIES:**

- Team player and active member of NASET, National level Cultural Fest at Kurukshetra University, Kurukshetra.
- Organized/Member Alumni Meet, National Institute of Technology, Srinagar.

**WORK STYLE:**

- Willing to think out of the box and move on to solve complex problems
- Strong learning appetite and adapts to new environments quickly
- Flexibility and agility
- Well-organized and passionate.