SANJEEV KUMAR
10 years Teaching and Publication Experience

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CAREER OBJECTIVE

Seeking a challenging career associated with a progressive organization that gives me a scope to apply and update my knowledge and skills.

ACHIEVEMENTS

I have work in Eduzphere Chandigarh publication. Under this I have made RRB,PSPCL,HSSC, SSC center exams books and complete material of electrical and electronics branch. I can solve solve the questions as a objective and with subjective approach also.

EXAMS QUALIFIED

- GATE-2010,2011, 2012 (ECE) qualified .
- GATE 2019(ELECTRICAL) qualified.
- NIELIT scientist exam qualified.
- Intelligence Bureau test qualified.

The following subjects I can handle comfortably.

- CIRCUIT THEORY.
- ELECTRONICS DEVICES & CIRCUIT.
- SIGNALS & SYSTEM
- ANALOG ELECTRONICS.
- DIGITAL ELECTRONICS.
- CONTROL SYSTEM.

- POWER ELECTRONICS
- MICROPROCESSOR
- MEASUREMENT
- ELECTRICAL MACHINE
- POWER SYSTEM
- COMMUNICATION SYSTEM
- ELECTRO MAGNETIC FIELD THEORY
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ACADEMIC PROFILE

	University/Board	Percentage
M.Tech(ECE)	Kurukshetra university	**70**
B.Tech(ECE)	Kurukshetra university	**65**
B.Tech(EE)	AMIE	**70**

PROJECTS ACCOMPLISHMENTS

1. Final Year M.Tech Research Project/Thesis

Design and Implementation of multiplier using LOOK AHEAD CARRY ADDER.

There are several techniques to realize adiabatic logic but most of them require compliment forms. In this work, a new adiabatic logic technique has been proposed which is capable of working with a single time varying supply voltage. The most attractive feature of the proposed technique is that there is no need of complementary inputs. The proposed adiabatic logic has been implemented by adding charging and discharging paths in the existing standard CMOS logic, using diodes and capacitors. Further, various logic circuits such as INVERTER, NAND, NOR, half adder and positive edge

triggered D-flip-flop have been implemented using the proposed adiabatic logic technique

TECHNICAL PROFICIENCY

Operating Systems: Windows XP/ 7/8
Languages: VHDL, Verilog.
Software known: XLINX, ModelSim–Altera, Questasim.

PAPER PUBLICATIONS

Efficient design for multiplication using modified BOOTH algorithm.in IJSRD vol 3 issue 4.

EXPERIENCE

- 3 years experience in Brain Tree GATE institute.
- 3 years experience in GATE INSIGHT.
- 4 years in EDUZPHERE INSTITUTE CHANDIGARH
- the Department of Electrical branch.

- Workes as a AP in Department of Electronics Engineering,JMIT RADAUR .(Kurukshera University) from 2008 to 2010

STRENGTHS

- Honest
- observer and learner
- Good communication skills
- Languages known: English , Hindi .

I undertake that the aforementioned information is true to the best of my knowledge and belief.