BRAHMA VASU GANDIKOTA

brahmavasu.gandikota@gmail.com

8309504922
9581322591

Education

Course	Year	School/college	Board/University	C.G.P.A
M.Tech(VLSI)	2011-2013	IIT-BOMBAY	Indian Institute of Technology	8.5
B.Tech(ECE)	2007-2011	IIIT-Nuzvid	RGUKT	8.28
Inter(M.PC)	2005-2007	IIIT-Nuzvid	RGUKT	9.35
S.S.C	2004-2005	Z.P.H.S-Poondla	School of Secondary Education	8.73

Technical Skills:

Operating Systems	:	Windows XP, Windows 7, Windows 8.1, Windows 10,Linux
Programming Languages	:	C
Database	:	MySQL
Package	:	MS-OFFICE

Non-Technical Skill

Excellent at communication and interaction, adapts easily into working environment; I am a passionate learner. I do my job sincerely. I make myself comfortable in a team, share my knowledge and learn from my team members and will guide the team when necessary.

Certifications

PROJECT LEAD AT NIT KURUKSHETRA.
Active Participation in all Extra-curricular activities.

Project:

A Bit-Plane Decomposition Matrix-Based VLSI Integer Transform Architecture for HEVC

Description: In this brief, a new very-large-scale integrated (VLSI) integer transform architecture is proposed for the High Efficiency Video Coding (HEVC) encoder. The architecture is designed based on the signed bit-plane transform (SBT) matrices, which are derived from the bit-plane decompositions of the integer transform matrices in HEVC. Mathematically, an integer transform matrix can be equally expressed by the binary weighted sum of several SBT matrices that are only composed of binary 0 or ±1. The SBT matrices are very simple and have lower bit width than the original integer transform in the form. The SBT matrices are also sparse and there are many zero elements. The sparse characteristic of SBT matrices is very helpful for saving the addition operators of SBT.

Languages: VHDL/Verilog HDL

Tools Used: Modelsim 6.4b, Xilinx ISE 13.2

Role: Project Lead

Experience:

- 4 years (September 2013 – October 2016) teaching experience at **GATE FORUM PRIVATE LTD** as a full time faculty(Asst Manager).I have taught the subjects of Networks, Signals and Systems, Analog Circuits and Digital Circuits.

- Currently working as full time faculty (January 2017 – March 2018) at **TIME PVT LTD** dealing the subjects of EDC, Analog Circuits and Digital Circuits.

Gate rank	Year	Gate Score	Gate Marks
AIR-30	2011	876	77
AIR-1536	2014	520	52

Personal Profile:

Name	:	BRAHMA VASU G
Father's Name	:	Srinivasarao G
Gender	:	male
Date of Birth	:	11/05/1989
Marital Status	:	Single
Nationality	:	Indian
Languages Known	:	English, Telugu
Phone no	:	9581322591
Hobbies & Interests	:	Listening music and Watching movies.

I hereby declare that all the details furnished above are true to the best of my knowledge and belief.

Brahma Vasu Gandikota